



The 24<sup>th</sup>  
**LSI 2021**  
**Design Contest in Okinawa**



# Installing Vivado 2019.1

■ Download Vivado Design Suite from the link below:

□ <https://japan.xilinx.com/support/download/index.html/content/xilinx/ja/downloadNav/vivado-design-tools/archive.html>

■ Install the downloaded file

# Opening Vivado

Vivado 2019.1

File Flow Tools Window Help Q Quick Access

VIVADO HLx Editions

XILINX

### Quick Start

- Create Project >
- Open Project >
- Open Example Project >

### Tasks

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

### Learning Center

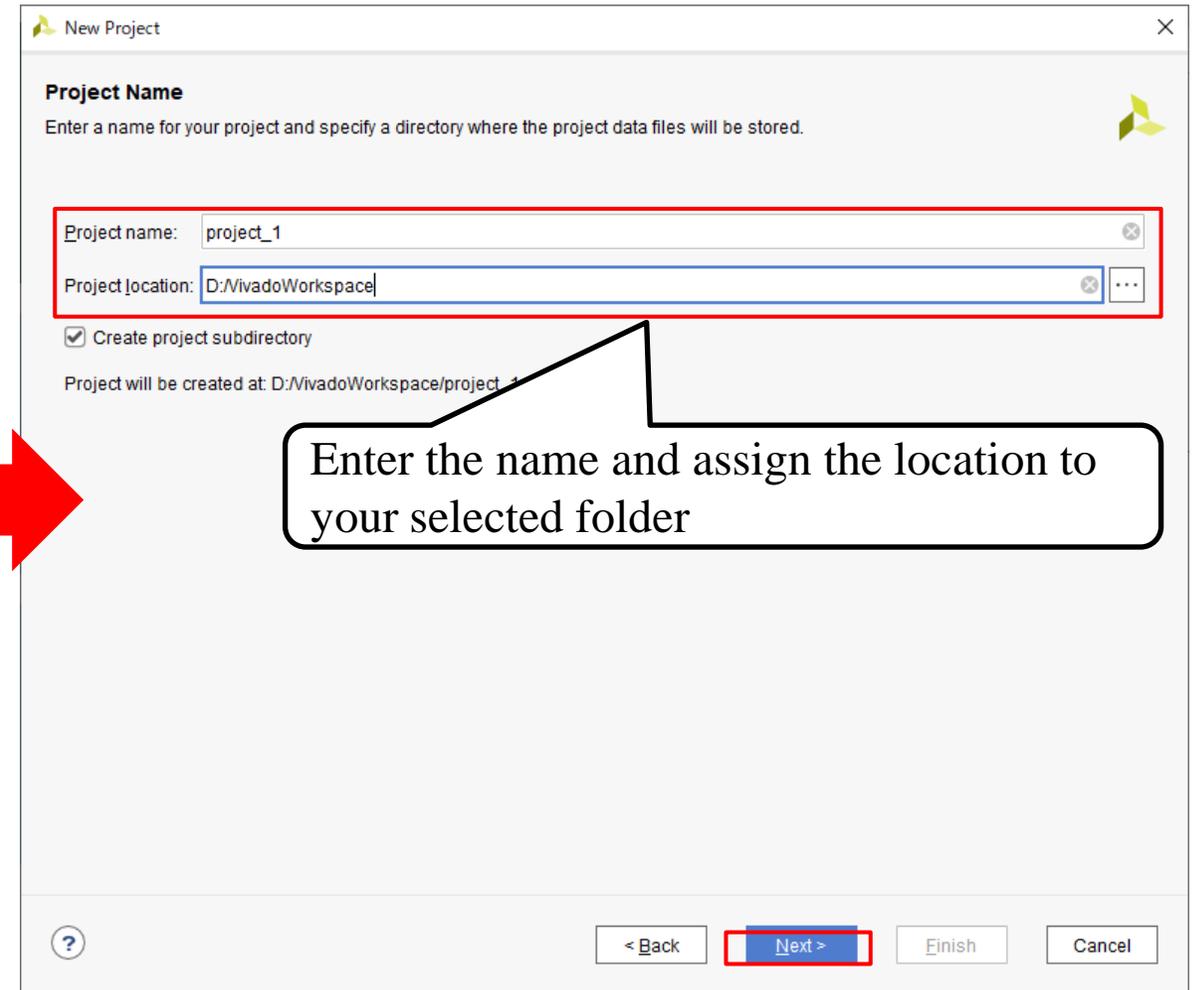
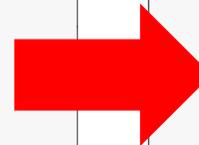
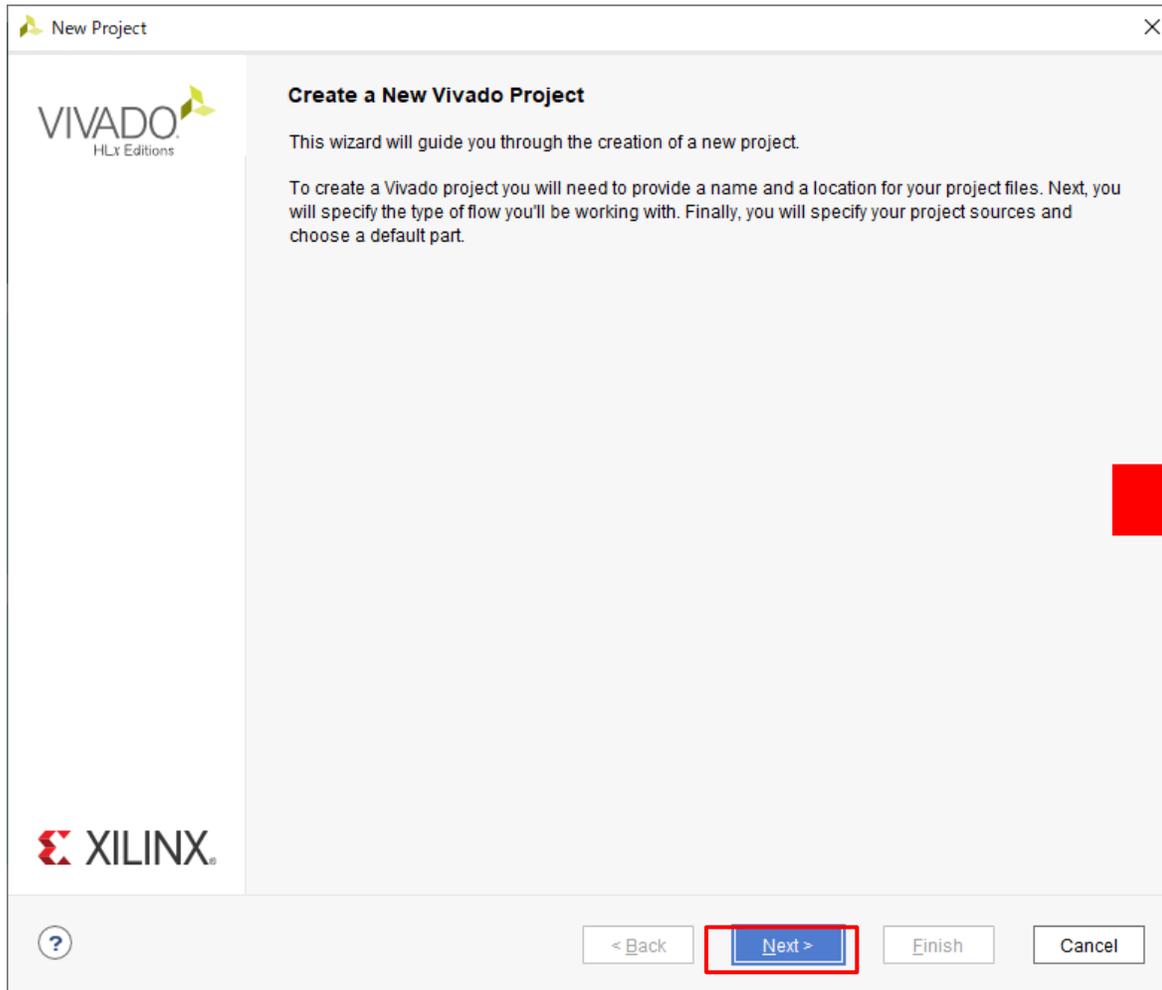
- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

#### Recent Projects

- LATCH  
D:/home/VIVADOWorkspace/seminar/LATCH
- DFF  
D:/home/VIVADOWorkspace/seminar/DFF
- rom  
D:/home/VIVADOWorkspace/seminar/rom
- comp\_EQ  
D:/home/VIVADOWorkspace/seminar/comp\_EQ
- comp\_GT  
D:/home/VIVADOWorkspace/seminar/comp\_GT
- project\_1multiplier  
D:/home/VIVADOWorkspace/seminar/project\_1multiplier
- twst2  
D:/home/VIVADOWorkspace/twst2
- shift  
D:/home/VIVADOWorkspace/seminar/shift
- test  
D:/home/VIVADOWorkspace/test/test

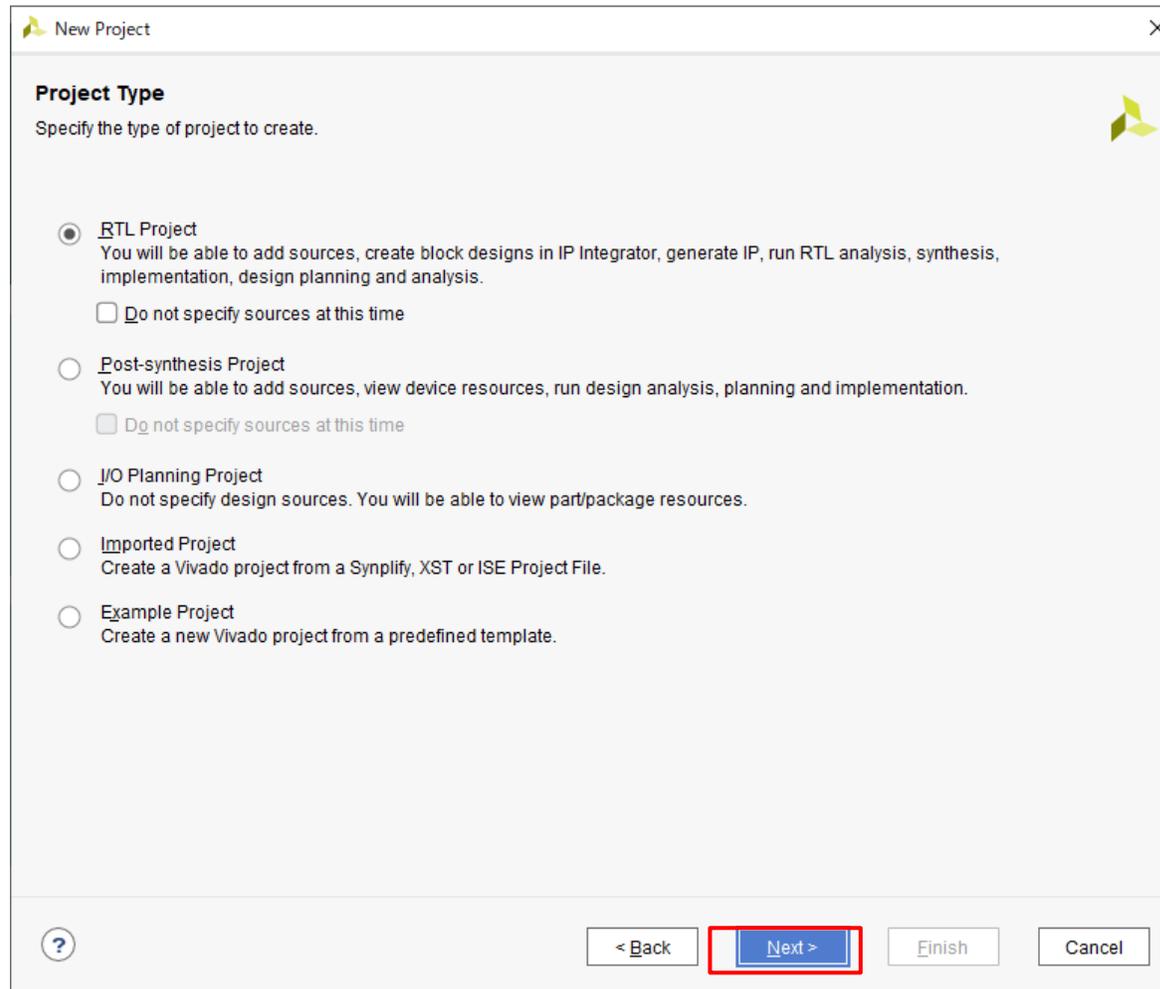
Tcl Console

# Create a new project



Enter the name and assign the location to your selected folder

# Create a new project



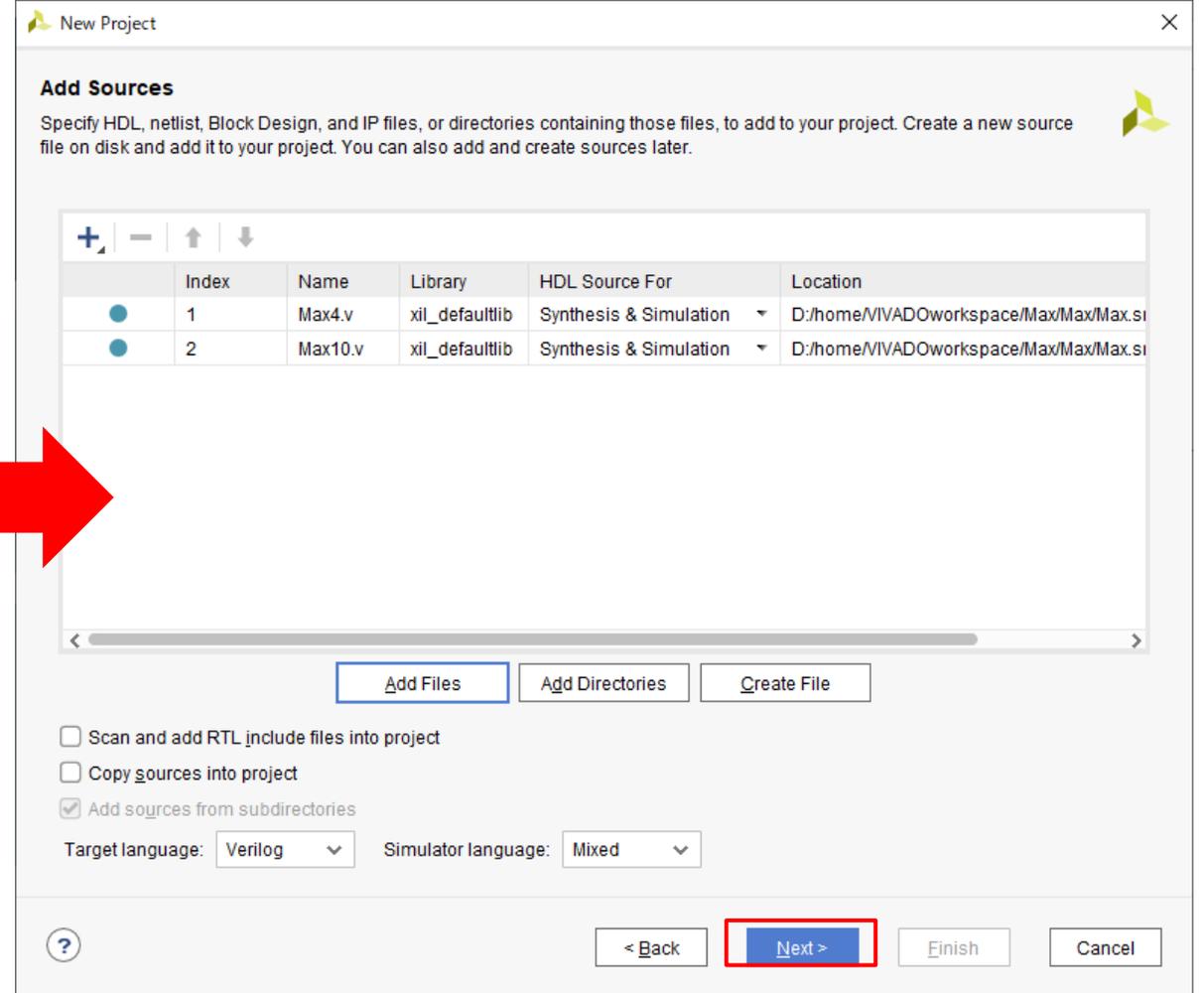
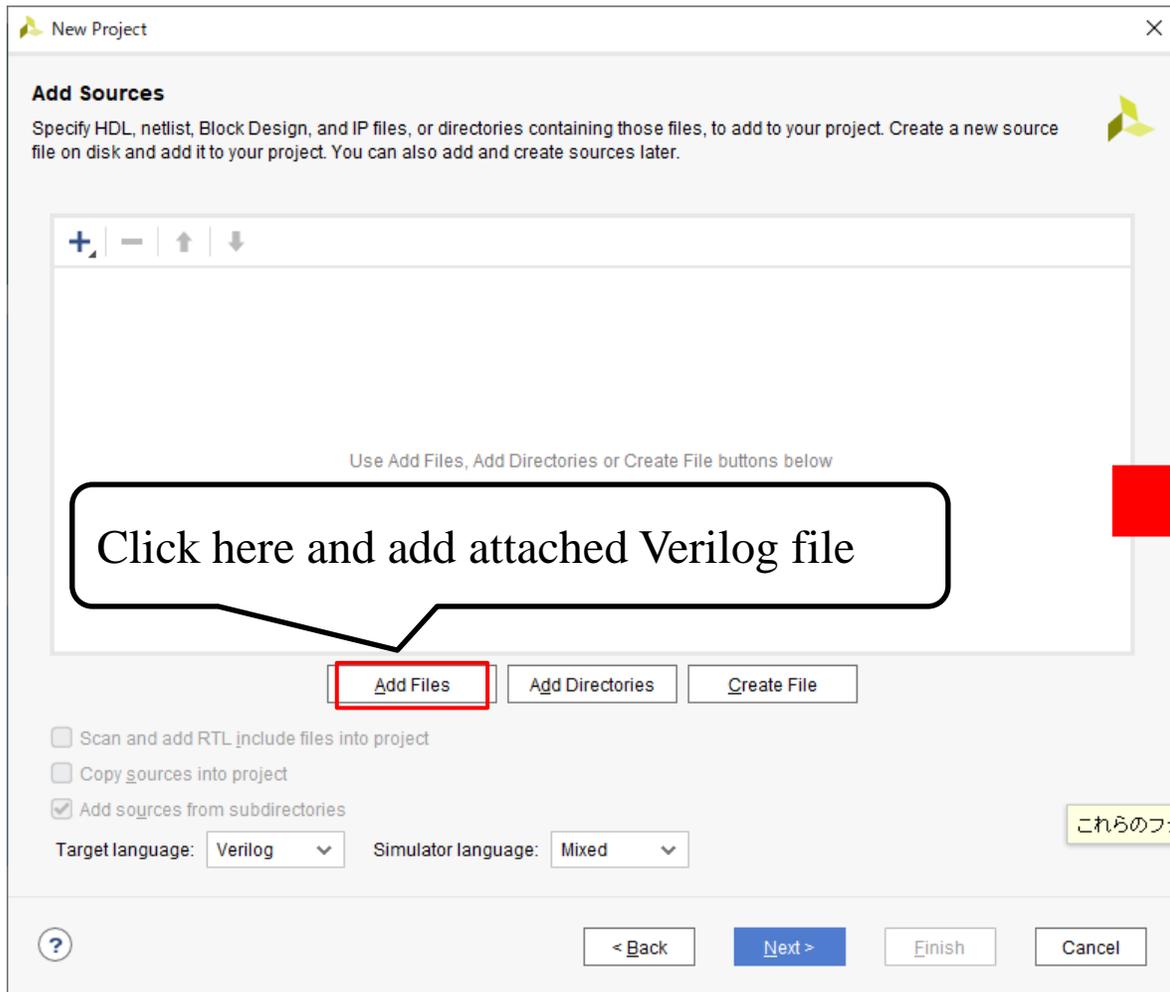
New Project

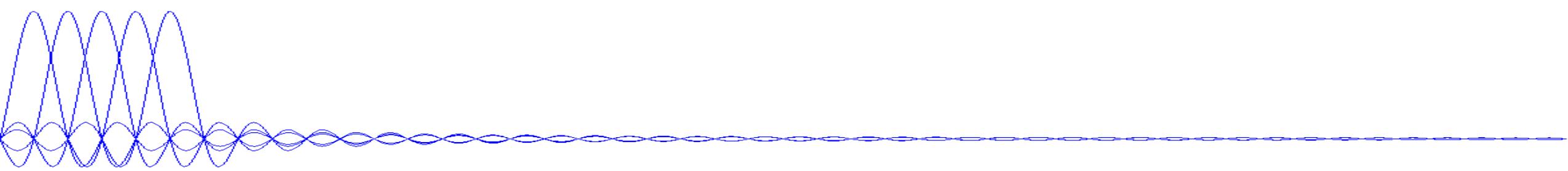
**Project Type**  
Specify the type of project to create.

- RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time
- Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time
- I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.
- Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project**  
Create a new Vivado project from a predefined template.

? < Back **Next >** Finish Cancel

# Add Verilog file





New Project ✕

**Add Constraints (optional)** 

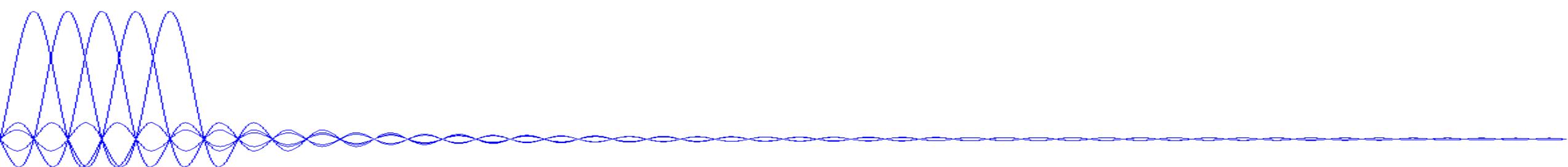
Specify or create constraint files for physical and timing constraints.



Use Add Files or Create File buttons below

Copy constraints files into project





New Project

### Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

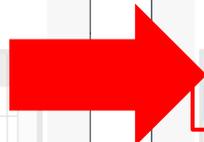
Category: All  
Family: All

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs
xc7vx415tffv1158-1	1158	350	257600	515200	880	0	2160
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800

Buttons: ? < Back Next > Finish Cancel

**Select part or boards. In this example, I use xc7z010clg400-1.**



New Project

### Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

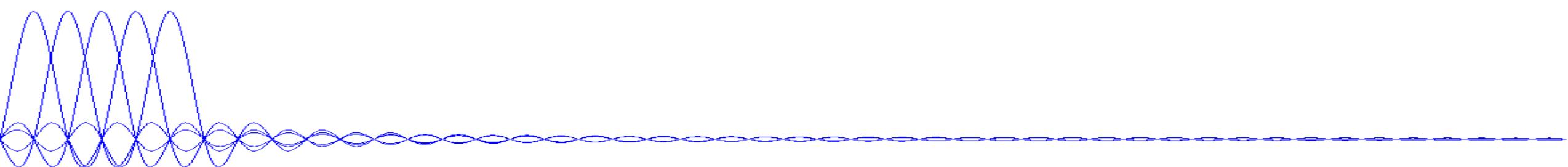
Reset All Filters

Category: All Package: All Temperature: All  
Family: All Speed: All Static power: All

Search: Q- xc7z010clg400-1 (1 match)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Ct
xc7z010clg400-1	400	100	17600	35200	60	0	80	0

Buttons: ? < Back Next > Finish Cancel



New Project

VIVADO<sup>®</sup>  
HLS Editions

### New Project Summary

- 1 A new RTL project named 'project\_1' will be created.
- 2 2 source files will be added.
- 3 No constraints files will be added. Use Add Sources to add them later.
- 4 The default part and product family for the new project:  
Default Part: xc7z010clg400-1  
Product: Zynq-7000  
Family: Zynq-7000  
Package: clg400  
Speed Grade: -1

XILINX<sup>®</sup>

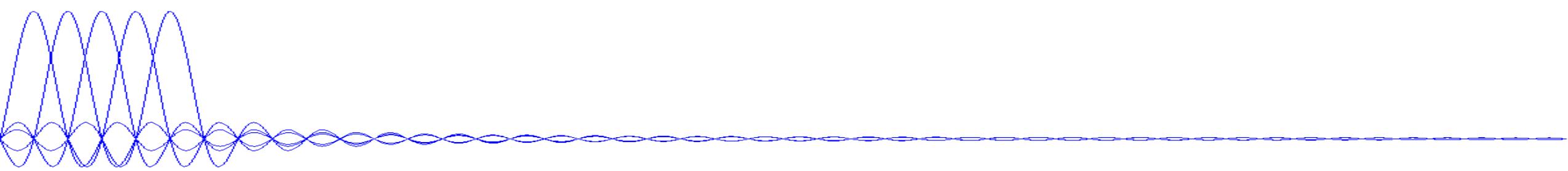
To create the project, click Finish

? < Back Next > **Finish** Cancel

# Add simulation file

The screenshot shows the Vivado 2019.1 Project Manager interface. The 'Sources' tab is active, displaying a tree view of project sources. A red box highlights the '+' icon in the Sources toolbar, with a red arrow pointing to it and a text box containing 'Click here'. The 'Project Summary' panel on the right shows project details such as name, location, and part number. The 'Design Runs' table at the bottom shows the status of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Run Strategy	Repo
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado



**Add Sources** [Close]

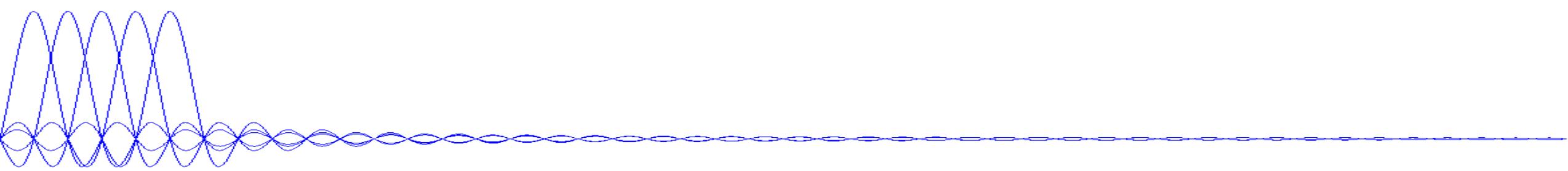
**VIVADO**  
HLx Editions

**Add Sources**  
This guides you through the process of adding and creating sources for your project

- Add or create constraints
- Add or create design sources
- Add or create simulation sources

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[Help] [Back] **Next >** [Finish] [Cancel]



**Add Sources**

**Add or Create Simulation Sources**

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set:

**Click here and add attached simulation file**

Scan and add RTL include files into project  
 Copy sources into project  
 Add sources from subdirectories  
 Include all design sources for simulation

**Add Sources**

**Add or Create Simulation Sources**

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set:

Index	Name	Library	Location
1	sim_max.v	xil_defaultlib	D:/home/VIVADOWorkspace/Max/Max/Max.srcs/sim_1/new

Scan and add RTL include files into project  
 Copy sources into project  
 Add sources from subdirectories  
 Include all design sources for simulation

シミュレーションのデザインソースすべてを含む

# Run simulation

1. Click here

2. Click here

Project Summary | **sim\_mux.v**

```
1 // timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 2020/10/13 16:16:47
7 // Design Name:
8 // Module Name: sim_max
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13
14 // Revision 0.01 - File Created
15 // Additional Comments:
16 //
17 //
18 //
19 //
20 //
21 //
22 //
23 module sim_max;
24
25 reg [16:0] in1, in2, in3, in4, in5, in6, in7, in8, in9, in10;
26 wire [16:0] max4, max10;
27
28 Max4 Max4(in1, in2, in3, in4, max4);
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Repo
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivad
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivad

# Get a simulation result

The screenshot displays the Vivado 2019.1 interface during a behavioral simulation. The main window is titled "SIMULATION - Behavioral Simulation - Functional - sim\_1 - sim\_max".

**Scope Table:**

Name	Design U...	Block Type
sim_r	sim_max	Verilog Modt
Ma: Max4		Verilog Modt
Ma: Max10		Verilog Modt
gbl	gbl	Verilog Modt

**Objects Table:**

Name	Value	Data Type
> in1[15:0]	000a	Array
> in2[15:0]	0014	Array
> in3[15:0]	001e	Array
> in4[15:0]	0028	Array
> in5[15:0]	0032	Array
> in6[15:0]	003c	Array
> in7[15:0]	0046	Array
> in8[15:0]	0050	Array
> in9[15:0]	005a	Array
> in10[15:0]	0064	Array
> max4	0028	Array
> max10	0064	Array

**Waveform Viewer:** Shows a signal trace for "sim\_mux.v" and "Untitled 2". The waveform displays the values of the objects over time, with a vertical yellow line indicating the current simulation time at 1,000,000 ps. The values for the objects are: in1[15:0] (000a), in2[15:0] (0014), in3[15:0] (001e), in4[15:0] (0028), in5[15:0] (0032), in6[15:0] (003c), in7[15:0] (0046), in8[15:0] (0050), in9[15:0] (005a), in10[15:0] (0064), max4[15:0] (0028), and max10[15:0] (0064).

**Tcl Console:**

```
INFO: [USF-XSim-98] XSim completed. Design snapshot 'sim_max_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB): peak = 929.266 ; gain = 0.000
```